METHOD FOR FORMING SHORT-CHANNEL TRANSISTORS

BACKGROUND OF THE INVENTION

Field of the invention

The present invention relates to a method for forming short-channel transistors, and more particularly to a method for forming transistors having short-channels using a damascene process.

Description of the Prior Art

As generally known in the art, in a transistor, since the length of a gate of N-channel Metal Oxide Semiconductor (NMOS) has become to be reduced below 0.14μm, a short channel effect (SCE) could not be gradually restricted. In order to restrict SCE, effective length of the channel should be basically increased. To this end, a reduction of dose rate in a lightly doped drain (LDD) region is effective.

However, the reduction of dose rate in an LDD region causes a degradation of a device by hot carrier effects because of a reduction of an effect of electric field relief, and causes a reduction of through-current because of an increase of resistance of LDD region, which makes it difficult to obtain

high performance products.

Meanwhile, in order to form an LDD region, an implantation of P or As ions can be conducted whereby a degradation of a device by hot carrier effects may be effectively prevented, but the horizontal and vertical extensions of an LDD by an implantation of P ions are large to a great extent because a diffusion by an annealing treatment is larger than that by As ion implantation.

Generally, dose rate of ion implants to sufficiently secure device performance (i.e., capable of reducing resistance of an LDD region) is above 3 X $10^{13}/cm^2$, which dose rate corresponds to high dose rate in a 0.14μm-class technology, causing a problem in that an SCE cannot be restricted.

Also, where As ions are adapted as implant impurities of an LDD region, diffusion by an annealing treatment is very smaller than that by P ion implantation, which effectively restricts an SCE. Nevertheless resistance of an LDD region can be reduced sufficient to secure through-current of a device, there is provided a problem in that hot carrier feature is worse than that in P implanted LDD region.

SUMMARY OF THE INVENTION

Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the prior art, and an object of the present invention is to provide a method for forming short-channel transistors having excellent characteristics through a reduction of short-channel effect.

In order to accomplish this object, there is provided a method for forming short-channel transistors, the method comprising the steps of: forming a first oxide layer and a sacrificial layer one after another on a semiconductor substrate and etching the sacrificial layer, thus forming a residual sacrificial layer pattern; conducting an ion implantation using the residual sacrificial layer pattern as a mask, thus forming an LDD ion-implant layer in the semiconductor substrate; forming the first spacers on both side walls of the residual sacrificial layer pattern; conducting an ion implantation using the residual sacrificial layer pattern and the first spacers as a mask, thus forming a source/drain ion-implant layer under the LDD ion-implant layer; forming a nitride layer and a second oxide layer one after another on the whole surface of the former resultant object and conducting an annealing treatment, thus forming source/drain regions; conducting chemical-mechanical polishing (CMP) processes to the extent that an upper surface of the residual sacrificial layer

pattern is exposed, and removing the residual sacrificial layer pattern through etching; forming the second spacers on side walls of a portion where the residual sacrificial layer patter is removed; conducting an ion implantation on the substrate between the second spacers, thus forming a punch-stop ion implant layer; etching the first oxide layer under the portion where the residual sacrificial layer pattern is removed, and forming a gate insulation layer; and forming a gate on the portion where the residual sacrificial layer pattern is removed.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

FIGS. 1A to 1E are end views showing a forming method of short-channel transistors of the present invention according to every process.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, a preferred embodiment of the present

invention will be described with reference to the accompanying drawings. In the following description and drawings, the same reference numerals are used to designate the same or similar components, and so repetition of the description of the same or similar components will be omitted.

FIGS. 1A to 1E are end views showing a forming method of short-channel transistors of the present invention according to every processes.

First, as shown in FIG. 1A, a first oxide layer 10 and a polysilicon sacrificial layer 20 are serially deposited on a semiconductor substrate 5, and a mask pattern 30 is formed thereon.

Then, as shown in FIG. 1B, the polysilicon sacrificial layer 20 is dry-etched using the mask pattern 30 to form a residual sacrificial layer 20a. An LDD ion implant layer 50 is formed on a source/drain ion implant layer to be subsequently formed, using an ion implantation process. Herein, the first oxide layer 10 is used as a buffer layer for ion implantation upon LDD ion implanting. Also, the first oxide layer can be used as an etch stopper layer.

Then, a first spacer layer (not shown) is deposited and etched on the whole surface thereof, thus forming the first spacers 40 on both side walls of the residual sacrificial layer

20a. The first spacer layer can be a nitride layer and the first spacers 40 can be composed of the same material as the second spacers to be formed at subsequent procedure.

Then, an ion implantation is conducted using the residual sacrificial layer 20a and the first spacers 40 as a mask, thus forming the source/drain ion implant layer 60 in the semiconductor substrate 5 under around the residual sacrificial layer. Herein, the source/drain ion implant layer 60 is formed under the LDD ion implant layer 50. Upon source/drain ion implanting, the first oxide layer 10 is used as a buffer layer for the ion implantation.

Then, as shown in FIG. 1C, on the whole surface of the former resultant object, a nitride layer 70 and a second oxide layer 80 are successively deposited. In this case, the second oxide layer 80 can be multi-layered.

Then, an annealing treatment is conducted to the LDD ion implant layer 50 and the source/drain ion implant layer 60, forming source/drain regions 55.

Then, as shown in FIG. 1D, CMP process is conducted to the second oxide layer 80 and the nitride layer 70, to the extent that the upper surface of the residual sacrificial layer 20a is exposed, so as to planarize the same, thus forming a second oxide layer 80a and a nitride layer 70a as shown in the drawing.

Then, wet-etching procedure is conducted to the whole surface of the former resultant object to completely remove the residual sacrificial layer 20a. Herein, upon etching the residual sacrificial layer 20a, the first oxide layer 10 is used as an etch stopper layer.

Then, a second spacer layer is deposited on the whole surface of the former resultant object and is etched, so that the second spacers 90 are formed on both side walls of the first spacers 40 where the residual sacrificial layer is removed. Herein, the second spacer layer can be a nitride layer and the second spacers 90 can be composed of the same material as the first spacers 40.

Then, an ion implantation is conducted between the source/drain regions 55 under a portion where a gate is formed later, thus forming a punch-stop ion implant layer 100. Herein, the punch-stop ion implant layer 100 can be adapted as a threshold-voltage Vth adjustment ion implant layer.

Then, as shown in FIG. 1E, the first oxide layer 10 under the gate-forming portion is wet-etched to form a first residual oxide layer 10a and a gate insulation layer 200.

Finally, a polysilicon layer is deposited on the whole surface of the structure including the gate-forming portion and is planarized to form a gate 300 in the gate-forming portion.

using the residual sacrificial layer 20a and the first spacers 40 as a mask, thus forming the source/drain ion implant layer 60 in the semiconductor substrate 5 under around the residual sacrificial layer.

According to the present invention as described above, in a forming method of transistors, short-channel transistors are formed using a spacer by a damascene method after previously forming the source/drain regions, thus reducing short channel effects (SCE) and a drain induced barrier lowering (DIBL) of the transistors, which makes it possible to fabricate transistors having excellent characteristics.

Also, by a forming method of transistors of the present invention, transistors having channels shorter than by other similar fabricating processes are provided.

Although preferred embodiments of the present invention have been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.